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Unit : **III**

Topic : **Characteristics of op-amp**

UNIT – III

Characteristics of op-amp

3.1 Ideal Characteristics of Op-Amp

An ideal Op-Amp would exhibit the following ideal electrical characteristic.

1. Infinite voltage gain A, so as to amplify very small signal.
2. Infinite input resistance R_i, so as to reduce loading effect of the preceding stage.
3. Zero output resistance R_O, so that output can drive an infinite number of other devices.
4. Zero output voltage when differential input voltage is zero.
5. Infinite bandwidth (BW), so that any frequency signals from 0 to infinite Hz can be amplified without any attenuation.
6. Infinite common mode rejection ratio (CMRR), so that the output common mode noise voltage is zero.
7. Infinite slew rate (SR), so that output voltage changes occur simultaneously with input voltage changes.

3.2 Practical Characteristics of Op-Amp

(i) Input Offset Voltage (V_{io})

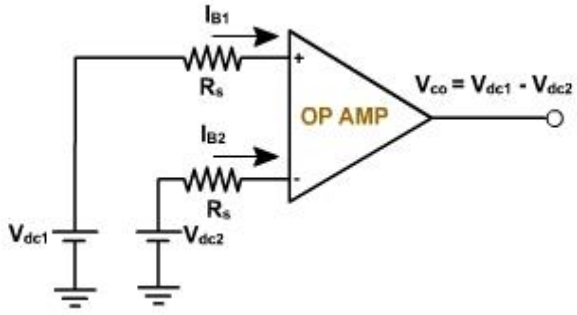

Figure 3.1 Defining input offset voltage

Input offset voltage is defined as the voltage that must be applied between the two input terminals of an Op-Amp to null or zero the output.

$$V_{io} = V_{dc1} - V_{dc2}$$

For a 741C Op-Amp the maximum value of V_{io} is 150μV.

(ii) Input Offset Current (I_{io})

The input offset current I_{io} is the difference between the currents flowing into inverting and non-inverting terminals of a balanced amplifier.

$$I_{io} = |I_{B1} - I_{B2}|$$

The input offset current (I_{io}) for the 741C is 200nA maximum.

(iii) Input Bias Current (I_B)

The input bias current I_B is the average of the current entering the input terminals of a balanced amplifier. It is given by:

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

The maximum value of input bias current (I_B) for IC 741C is 500 nA.

(iv) Differential Input Resistance (R_i)

Differential input resistance (R_i) is the equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal is grounded.

For the IC 741C the input resistance (R_i) is relatively high 2MΩ.

(v) Input Capacitance (C_i)

Input capacitance (C_i) is the equivalent capacitance that can be measured at either the inverting and non-inverting terminal with the other terminal connected to ground.

A typical value of Input capacitance (C_i) is 1.4pf for the 741C.

(vi) Input Voltage Range

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and non-inverting input terminals.

For the 741C, the range of the input common mode voltage is ± 13V maximum. This means that the common mode voltage applied at both input terminals can be as high as +13V or as low as –13V.

(vii) Output Voltage Swing

The output voltage swing is the maximum unclipped peak to peak output voltage that an Op-Amp can produce. The output voltage never exceeds these limits for a given supply voltages $+V_{CC}$ and $-V_{EE}$.

For a 741C it is ± 13 V.

(viii) Large Signal Voltage Gain (A_d)

Since the Op-Amp amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

$$A_d = \frac{v_o}{v_{id}}$$

For 741C is voltage gain is 200,000 typically.

(ix) Supply voltage Rejection Ratio (SVRR)

SVRR is the ratio of the change in the input offset voltage to the corresponding change in power supply voltages. SVRR is expressed in µV/V, it can be defined as

$$SVRR = \frac{\Delta V_{io}}{\Delta V}$$

Where ΔV is the change in the input supply voltage and ΔV_{io} is the corresponding change in the offset voltage.

For the 741C, SVRR = 150 µ V / V.

(x) Slew Rate (SR)

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions. It is expressed in volts / µ sec.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} V/\mu s$$

For the 741C the slew rate is low 0.5 V / µs.

(xi) Common Mode Rejection Ratio (CMRR)

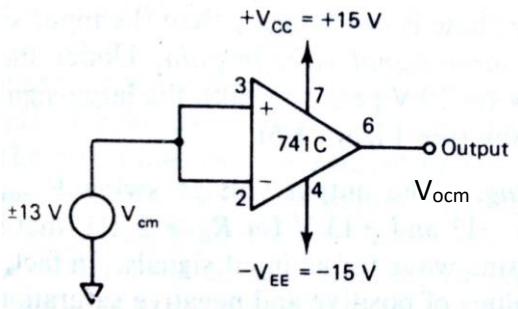

Figure 3.2 common mode configuration

CMRR is defined as the ratio of the differential voltage gain A_d to the common mode voltage gain A_{cm}.

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

The differential gain A_d is large signal voltage gain. The common mode gain A_{cm} is determined from the circuit.

$$A_{cm} = \frac{V_{ocm}}{V_{cm}}$$

For the 741C, the value of CMRR is 90 dB typically.

(xi) Unity Gain Bandwidth Product (UGB)

The Unity gain-bandwidth (UGB) is the bandwidth of the op-amp when the voltage gain is unity (1).

For 741C, its practical value is approximately 1MHz.

(xii) Output Resistance (R_O)

Output resistance (R_O) is the equivalent resistance that can be measured between the output terminal of the Op-Amp and the ground.

It practical value is 75 ohm for the IC 741C.

3.3 Input Bias Current

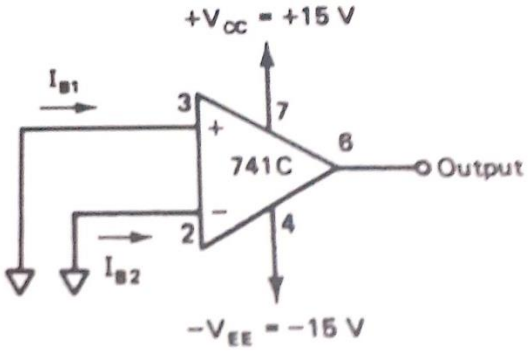

Figure 3.3 Input bias current in op-amp

The input bias current I_B is defined as the average of the two input bias current I_{B1} and I_{B2}, as shown in figure 3.3; that is,

$$I_B = \frac{I_{B1} + I_{B2}}{2} \quad (1)$$

Where I_{B1} = dc bias current flowing into the non-inverting input

I_{B2} = dc bias current flowing into the inverting input

As shown in figure 3.3, both input terminals are grounded so that no input voltage is applied to the op-amp. The value of input bias current I_B is very small, for IC 741C I_B is 500nA maximum at supply voltages = ±15 V dc. Even though very small, the input bias current I_B can cause a significant output offset voltage in circuits using large feedback resistors. It is necessary to minimize the input bias current.

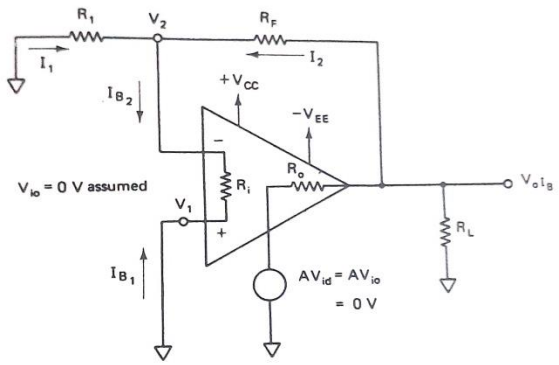

Figure 3.4 Output offset voltage due to input bias current

As shown in figure 3.4, input bias current I_{B1} and I_{B2} are flowing into the non-inverting and inverting input terminals respectively. The non-inverting input terminal is connected to ground therefore $V_1 = 0V$. The controlled voltage source $AV_{io} = 0V$ since $V_{io} = 0V$ is assumed. Since output resistance R_o is negligible small, the output terminal essentially at ground potential. Thus resistor R_1 and R_F are in parallel and bias current I_{B2} flowing through them. Therefore voltage at the inverting terminal is

$$V_2 = (R_1 \parallel R_F) I_{B2}$$

$$V_2 = \frac{R_1 R_F}{R_1 + R_F} I_{B2} \tag{2}$$

Writing KCL on node V_2, we get

$$I_1 + I_2 = I_{B2}$$

$$\frac{0 - V_2}{R_1} + \frac{V_{oIB} - V_2}{R_F} = \frac{V_2}{R_i} \tag{3}$$

Where V_{oIB} = output offset voltage due to input bias current

R_i = input resistance of the op-amp

Rearranging equation (3) we get,

$$\frac{V_{oIB}}{R_F} = V_2 \left(\frac{1}{R_1} + \frac{1}{R_F} + \frac{1}{R_i} \right)$$

Since R_i is very large (ideally infinite) $1/R_i = 0$. Therefore

$$\frac{V_{oIB}}{R_F} = V_2 \frac{R_1 + R_F}{R_1 R_F} \tag{4}$$

Substituting the value of V_2 from equation (2) to equation (4) we have

$$V_{oIB} = \frac{R_1 R_F}{R_1 + R_F} I_{B2} \frac{R_1 + R_F}{R_1}$$

$$\boxed{\boldsymbol{V_{oIB} = R_F I_{B2} = R_F I_B}} \tag{5}$$

According to equation (5), the amount of offset voltage V_{oIB} is a function of feedback resistor RF. The amount of V_{oIB} can be increased by the use of relatively large feedback resistor. To eliminate or reduce V_{oIB}, some scheme has to be devising at input by which voltage V_1 can be made equal to V_2. From equation (2), we have,

$$V_2 = R_p I_{B2} \quad (6)$$

Where $R_p = \frac{R_1 R_F}{R_1 + R_F}$

To made $V_1 = V_2$, some specific resistance ROM has to be implant at the non-inverting input terminal such that

$$V_1 = R_{OM} I_{B1} \quad (7)$$

From equation (6) and (7)

$$R_{OM} I_{B1} = R_p I_{B2}$$

Now if the current IB1 and IB2 are equal

$$R_{OM} = R_p$$

Or $\boxed{R_{OM} = \frac{R_1 R_F}{R_1 + R_F}}$

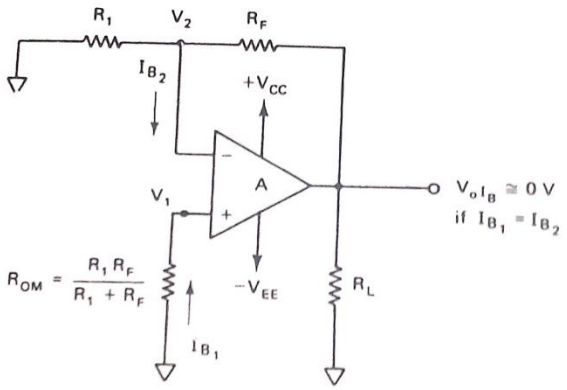

Figure 3.5 R_{OM} reduces output offset voltage V_{oIB}

However R_{OM} may not completely eliminate the output offset voltage V_{oIB}, but it can minimize the amount of output offset voltage V_{oIB}. Therefore the R_{OM} is referred as the offset minimizing resistor.

3.4 Input Offset Current

We have discussed in last section that the use of R_{OM} in series with the non-inverting input terminal reduces the effect of output offset voltage V_{oIB} due to input bias current I_B. The value of R_{OM} was derived based on the assumption that the input bias currents I_{B1} and I_{B2} are equal. In practice, these currents are not equal because of internal imbalances

in the op-amp circuitry. The input offset current is used to indicate the degree of mismatching between these two currents.

The input offset current I_{io} is defined as the algebraic difference the two input bias currents I_{B1} and I_{B2}.

$$\boldsymbol{I_{io} = I_{B1} - I_{B2}} \qquad (8)$$

For IC 741C maximum value of input offset current I_{io} = 200nA.

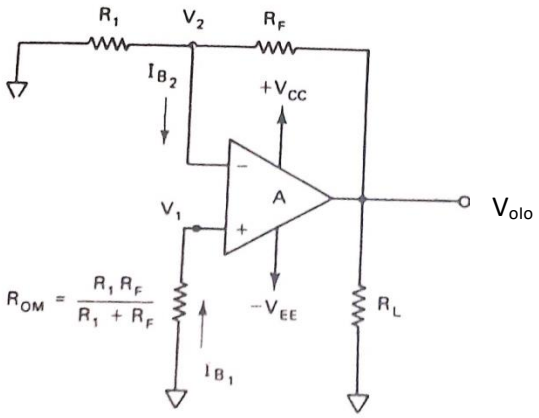

Figure 3.6 Output offset voltage V_{oio} caused by I_{io}

From the figure 3.6, it is clear that the voltages V_1 and V_2 are the function of I_{B1} and I_{B2} respectively, for the given value of R_1 and R_F.

$V_1 = R_{OM}\, I_{B1}$

$V_2 = R_p\, I_{B2}$

Where $R_{OM} = R_p = \frac{R_1 R_F}{R_1 + R_F}$

Applying superposition theorem to find V_{oIb}

$V_{oIB2} = -R_F\, I_{B2}$ (from equation (5) (9)

Negative sign is used because V_2 is the voltage the inverting input terminal.

$$V_{oIB1} = V_1 \left(1 + \frac{R_F}{R_1}\right) \qquad (10)$$

Where V_1 = voltage at the non-inverting input terminal

Substituting the value of V1 from equation (2) into equation (10) we get,

$$V_{oIB1} = R_{OM} I_{B1} \left(1 + \frac{R_F}{R_1}\right) = \frac{R_1 R_F}{R_1 + R_F} I_{B1} \frac{R_1 + R_F}{R_1}$$

$$V_{oIB1} = R_F \, I_{B1} \qquad (11)$$

From equation (9) and (11) we get,

$$V_{oIB} = V_{oIB1} + V_{oIB2} = R_F \, I_{B1} - R_F \, I_{B2}$$

$$= R_F \, (I_{B1} - I_{B2})$$

$$\boxed{V_{oIB} = R_F \, V_{oIo}} \qquad (12)$$

3.5 Total Output Offset Voltage

As we know that, the output offset voltage V_{oo} caused by input offset voltage V_{io} could be either positive or negative with respect to ground. Similarly the output offset voltage V_{oIB} caused by input bias current IB could also be either positive or negative with respect to ground. If these output offset voltage are of different polarities the resultant output offset voltage will be little. On the other hand, if both of these output offset voltages are of same polarity, the maximum amplitude of the total output offset would be,

$$V_{ooT} = V_{oo} + V_{oIB}$$

$$V_{ooT} = \left(1 + \frac{R_F}{R_1}\right) V_{io} + (R_F) I_B \qquad (13)$$

After compensation of input bias current, the total offset voltage can be given as

$$V_{ooT} = V_{oo} + V_{io}$$

$$V_{ooT} = \left(1 + \frac{R_F}{R_1}\right) V_{io} + (R_F) I_{io} \qquad (14)$$

3.6 Thermal Drift

After compensation of input offset voltages, input offset current and input bias current, parameters V_{io}, I_{io} and I_B are constant. However in practice the value of V_{io}, I_{io} and I_B vary with:

1. Change in temperature
2. Change in supply voltages: $+V_{CC}$ and $-V_{EE}$
3. Time

The average rate of change of input offset voltage per unit change in temperature is called ***thermal drift*** and it is denoted by $\frac{\Delta V_{io}}{\Delta T}$. It is expressed in μV/°C. It is assumed that input offset voltage and current is zero at room temperature (25°C). If the temperature changes from 25°C denoted by $\boldsymbol{\Delta T}$ the input offset voltage and current changes.

For LM101A op-amp the average temperature coefficient of input offset voltage is $\frac{\Delta V_{io}}{\Delta T} = \boldsymbol{15\,\mu V/}$°C maximum. And the average temperature coefficient of input offset current is $\frac{\Delta I_{io}}{\Delta T} = \boldsymbol{200\,pA/}$°C maximum.

3.6.1 Error Voltage

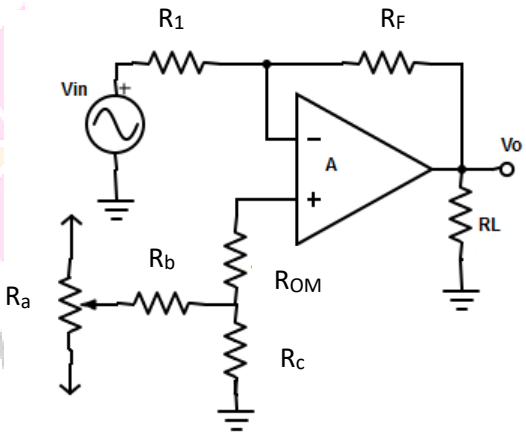

Figure 3.7 completely compensated inverting amplifier

Let us consider completely compensated inverting amplifier as shown in figure 3.7. Assume that amplifier is nulled at room temperature (25°C); that is the effect of V_{io} and I_{io} is reduced to zero. The value of V_{io} and I_{io} changes (drift) with temperature, hence any change in the value of V_{io} and I_{io} results in change in the total output offset voltage.

The average change in total output offset voltage per unit change in temperature is given by:

$$\frac{\Delta V_{ooT}}{\Delta T} = \left(1 + \frac{R_F}{R_1}\right)\frac{\Delta V_{io}}{\Delta T} + (R_F)\frac{\Delta I_{io}}{\Delta T} \qquad (15)$$

Where $\Delta V_{ooT}/\Delta T$ is the average change in total output offset voltage per unit change in temperature, in $\mu V/°C$. Multiplying both side by ΔT in equation (15) we get,

$$\Delta V_{ooT} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta T}\right)\Delta T + (R_F)\left(\frac{\Delta I_{io}}{\Delta T}\right)\Delta T \qquad (16)$$

This maximum possible change in total output offset voltage ΔV_{ooT} is known as ***error voltage*** denoted by E_v. Therefor equation (16) is rewritten as:

$$E_v = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{\Delta V_{io}}{\Delta T}\right)\Delta T + (R_F)\left(\frac{\Delta I_{io}}{\Delta T}\right)\Delta T \qquad (17)$$

Since error voltage could be either positive or negative, thus expression for output voltage for the inverting amplifier shown in figure 3.7 may be written as:

$$\boldsymbol{v_o = \left(-\frac{R_F}{R_1}\right)v_{in} \pm E_v} \qquad (18)$$

3.7 Effect of Variation in Power Supply Voltage on Offset Voltage

Operational amplifier uses $+V_{CC}$ and $-V_{EE}$ for its operation. These voltages may change as a result of poor regulation and filtering. A poorly regulated power supply gives different values depending on the size and type of load connected to it. On the other hand a poorly filtered power supply has a ripple voltage of some specific dc level.

For a given op-amp any change in the value of the supply voltages result in a change in input offset voltage. The change in input offset voltage caused by variation in the supply voltages is referred as ***Supply Voltage Rejection Ratio (SVRR), Power Supply Rejection Ration (PSRR) or Power Supply Sensitivity***. These terms are expressed either in ***μV/V*** or in decibels. For op-amp μA741 SVRR is 150μV/V maximum. Note that lower the value of SVRR in ***μV/V,*** the performance of op-amp is better. In fact ideally the value of SVRR in ***μV/V*** should be zero.

For a well-compensated op-amp the output offset voltage is given by:

$$V_{oo} = \left(1 + \frac{R_F}{R_1}\right)V_{io} \qquad (19)$$

The average change in output offset voltage V_{oo} per unit change power supply voltage can be

$$\frac{\Delta V_{oo}}{\Delta V} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_{io}}{\Delta V}\right) \qquad (20)$$

Multiplying both side in equation (20) by ΔV, we get

$$\boxed{\Delta V_{oo} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_{io}}{\Delta V}\right)\Delta V} \qquad (21)$$

Where ΔV_{oo} = change in output offset voltage (volts)

ΔV = change in supply voltages $+V_{CC}$ and $-V_{EE}$

$\frac{V_{io}}{\Delta V}$ = Supply voltage rejection ration (μV/V)

Remember that ΔV_{oo} is a dc voltage, and it could be either positive or negative.

3.8 Slew Rate

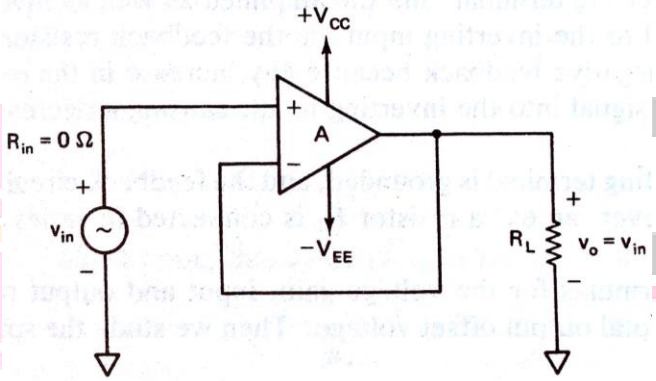

Figure 3.8 Calculation of Slew Rate

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions. It is expressed in volts / μ sec.

$$SR = \frac{dV_o}{dt}\Big|_{max} \; V/\mu s$$

Let $v_{in} = V_p \sin(\omega t)$

For a voltage follower $v_o = v_{in} = V_p \sin(\omega t)$

The rate of change of output is

$$\frac{dv_o}{dt} = V_p \omega \cos \omega t$$

The maximum rate of change of the output occurs when ***cos (ωt)*** equals to 1.

$$\left.\frac{dv_o}{dt}\right| max = V_p \omega$$

$\boldsymbol{SR = 2\pi f\, V_p}$ volts/sec

Or $\boldsymbol{SR = \frac{2\pi f V_p}{10^6}\ volts/\mu Sec}$

Where SR = slew rate (volts/µsec)

f = Frequency of input signal (Hz)

V_p = peak value of output sine wave (volts)